USSN 09/964,472
Art Unit: 2812

Remarks

A marked up version of the amendments is submitted herewith.

By their amendments, the applicants have amended the abstract to conform to the requirements. As the Examiner will note, one aspect of the invention is that a number of different types of integrated circuit can be made by selecting a sequence of mask steps from a predefined common set. This aspect has been referred to in the abstract and gives readers sufficient information to determine whether detailed reference to the specification is necessary.

Claim 1 has been amended to avoid the use of the omission step. Claim 1 now defined the common set as a Markush group, and specifies that a sequence is selected from the group which consists of at least the non-omitted steps, and at least one of the steps that were specified as being omissible. It is believed that the amended wording should be acceptable since the invention is claimed in a positive manner.

Claim 18 has been cancelled.

The objection to claim 19 is respectfully traversed since the claim is in the form of a single sentence, which incorporates a table comprising a detailed listing of the steps. The listing does not however comprise multiple sentences. It is respectfully submitted that claim 19 is clear under 35 USC 112 because it defines in detail the nature of each of the mask steps of the predefined common set.

It is believed that this application is in condition for allowance and reconsideration and allowance are respectfully requested.

Respectfully submitted

BY: _____
Richard J. Mitchell
Reg. No. 34519

Marks & Clerk
P.O.Box 957, Station B
Ottawa, Ontario
Canada K1P 5S7
(613) 236-9561

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Marked Up version showing amendments.

-- A process for making ~~an~~ integrated circuits of different type is described wherein sequence of mask steps is applied to a substrate or epitaxial layer of p-type material. The sequence ~~consists of the following steps~~is chosen from a predefined common set of mask steps according to the particular type of integrated circuit to be fabricated. In this way, various types of integrated circuit can be fabricated in a most efficient manner.~~:~~

~~(1) applying a first mask and forming at least one N-well in said p-type material therethrough;~~

~~(2) applying a second mask and forming an active region therethrough;~~

~~(3) applying a third mask and forming a p-type field region therethrough;~~

~~(4) applying a fourth mask and forming a gate oxide therethrough;~~

~~(5) applying a fifth mask and carrying out a p-type implantation therethrough;~~

~~(6) applying a sixth mask and forming polysilicon gate regions therethrough;~~

~~(7) applying a seventh mask and forming a p-base region therethrough;~~

~~(8) applying an eighth mask and forming a N-extended region therethrough;~~

~~(9) applying a ninth mask and forming a p-top region therethrough;~~

~~(10) applying a tenth mask and carrying out an N+ implant therethrough;~~

~~(11) applying an eleventh mask and carrying out a P+ implant therethrough;~~

~~(12) applying a twelfth mask and forming contacts therethrough;~~

~~(13) applying a thirteenth mask and depositing a metal layer therethrough;~~

~~(14) applying a fourteenth mask and forming vias therethrough;~~

~~(15) applying a fifteenth mask and depositing a metal layer therethrough; and~~

~~(16) applying a sixteenth mask and forming a passivation layer therethrough. Up to any three of mask steps 4, 7, 8, and 9 may be omitted depending on the type of integrated circuit.~~

1(Amended). A process for making an different types of integrated circuit, comprising:

a) providing a substrate or epitaxial layer of p-type material; and

b) ~~applying~~ selecting a sequence of mask steps ~~as follows~~from a predefined set of mask steps selected from the group consisting of:

(1) applying a first mask and forming at least one N-well in said p-type material therethrough;

(2) applying a second mask and forming an active region therethrough;

(3) applying a third mask and forming a p-type field region therethrough;

(4) applying a fourth mask and forming a gate oxide therethrough;

(5) applying a fifth mask and carrying out a p-type implantation therethrough;

(6) applying a sixth mask and forming polysilicon gate regions therethrough;

(7) applying a seventh mask and forming a p-base region therethrough;

(8) applying an eighth mask and forming a N-extended region therethrough;

(9) applying a ninth mask and forming a p-top region therethrough;

(10) applying a tenth mask and carrying out an N+ implant therethrough;

(11) applying an eleventh mask and carrying out a P+ implant therethrough;

(12) applying a twelfth mask and forming contacts therethrough;

(13) applying a thirteenth mask and depositing a metal layer therethrough;

(14) applying a fourteenth mask and forming vias therethrough;

(15) applying a fifteenth mask and depositing a metal layer therethrough; and

(16) applying a sixteenth mask and forming a passivation layer therethrough; and

wherein said sequence consists of at least said mask steps 1 to 3, 5, 6, and 10 to 16 and at least one ~~up to any~~ of said ~~three of~~ mask steps 4, 7, 8, and 9 ~~may be omitted~~ depending on the type of integrated circuit; and

performing said selected sequence of mask steps in numerical order.